SAMSUNG

S5L2010

DPF PROCESSOR

S5L2010D S5L2010X01-X080
S5L2010A S5L2010X01-X081
S5L2010L S5L2010X02-X080

DPF PROCESSOR

USER'S MANUAL

Revision 1.0

Email:Tech@fosvos.com
HotTel:+86-21-58998693

PRODUCT OVERVIEW

INTRODUCTION

The S5L2010 DPF SOC is designed to provide a cost-effective, low power and high performance Digital Photo Frame. To reduce total system cost, the S5L2010 integrates the following functions: an advanced Audio/Video decoder, a control CPU with 4KB/4KB instruction/data separated caches. Also S5L2010 supports various I/F's, USB2.0 OTG, TCON, ATA, IIC, IIS, IR, SIO, SPDIF OUT, general purpose I/O Ports, RTC, Jog-shuttle, 2-channel UART with handshake, DVB-T I/F, 10-bit ADC for Touch-screen, 3-channel 10-bits Video DAC, 5-channel Timer with PWM, 2-channel audio PWM out and 3-PLLs for clock generation.

The S5L2010 is fabricated in a standard 65nm CMOS technology. Its low power and static design is suitable for power-sensitive applications.

The S5L2010 is built around the ARM9 CPU core: The ARM9 cached processor provides a complete optimal performance CPU subsystem, including ARM946E-S RISC integer CPU, 4KB instruction/data separated caches, with an AMBA bus interface. The ARM946E-S core executes both the 32-bit ARM and 16-bit Thumb instruction sets, allowing the user to trade off between high performance and high code density. It is binary compatible with ARM9TDMI, ARM10TDMI, and StrongARM processors, and is supported by a wide range of tools, operating systems, and application software.

S5L2010D (For Digital TFT, 128pin) S5L2010X01-X080

S5L2010A (For Analogur panel, 128pin) S5L2010X01-X081

S5L2010L (For digital TFT, 128pin, Photo only) S5L2010X02-X080

S5L2010F (For both Digital and analogue panel, 160pin)

ARCHITECTURE

- 176MHz ARM9 (ARM946E-S, 4KB/4KB separated cache)
- MPEG Video stream decoder : MPEG1, MPEG2(MP@ML), MPEG4-ASP
- Audio stream decoder (Audio DSP: CalmMAC24)
- Format conversion, Scaling, NTSC/PAL encoder
- Graphic processor (Multiple windows, BitBLT)
- 16-bit Unified Memory Architecture for SDR
- On-chip clock generator with PLL
- Core peripherals (UART, I2S, I2C, SPDIF, IR, SPI, GPIO, USB2.0 OTG etc.)
- Memory card interfaces (MstickPro, SDC, MMC, NAND, xD, CF)

VIDEO	
Decoding Standard	MPEG-1 (ISO/IEC 11172-2), MPEG-2 (ISO/IEC 13818-2), MPEG4-ASP, M-JPEG
Source Resolutions	Decoding : Up to 960x600, Display : Up to 1024x768
Video File Format	MPEG1, MPEG4 and AVI
Graphic Processor	Multi Windows / colour modes, mixing, cursor, scaling, BitBLT
Video Post Processing	Contrast, Brightness, Hue, Sharpness Enhancement
AUDIO	
Decoding Standard	MPEG-1 and MPEG-2, Layer1, 2, 3(MP3), WMA, AAC, and OGG
Input/Output Channel	2-ch PWM Audio output, SPDIF output, 3-channel I2S Output, 1-ch I2S Input
JPEG	
Decoding Standard	Decoded ITU-T.81 (ISO/IEC 10918-1) compliant process
Deciding size	65536x65536 (tested 16384x16384)
Decoding speed	Max 57Mpixel/sec
Image decoding : others	BMP, GIF, TIFF, PNG
LCD I/F	
LCD I/F	Analog/Digital LCD I/F, CPU I/F
TCON I/F	Analog/Digital DDI I/F
SYSTEM	
Peripheral Interface	UART, IR, I2C, I2S, SPI, SPDIF, USB2.0OTG, DVB-T Channel I/F 10-bit ADC(for Touch Screen), RTC
Memory Card Interface	MstickPro, SDC, MMC, NAND, xD, CF, MicroDrive
Memory Interface	SDRAM I/F(16-bit Data Bus), Serial Flash I/F(1bit/2bit), EDO DRAM I/F(4bit/8bit)
PHYSICAL	
Operating Voltage	3.3V I/O, 1.2V core
Clock Frequencies	Input Frequency = 24MHz, ARM : up to 176MHz, SDRAM : up to 132MHz
Packaging	160-LQFP-2424, 128-eTQFP-1414

Email:Tech@fosvos.com
HotTel:+86-21-58998693

BLOCK DIAGRAM

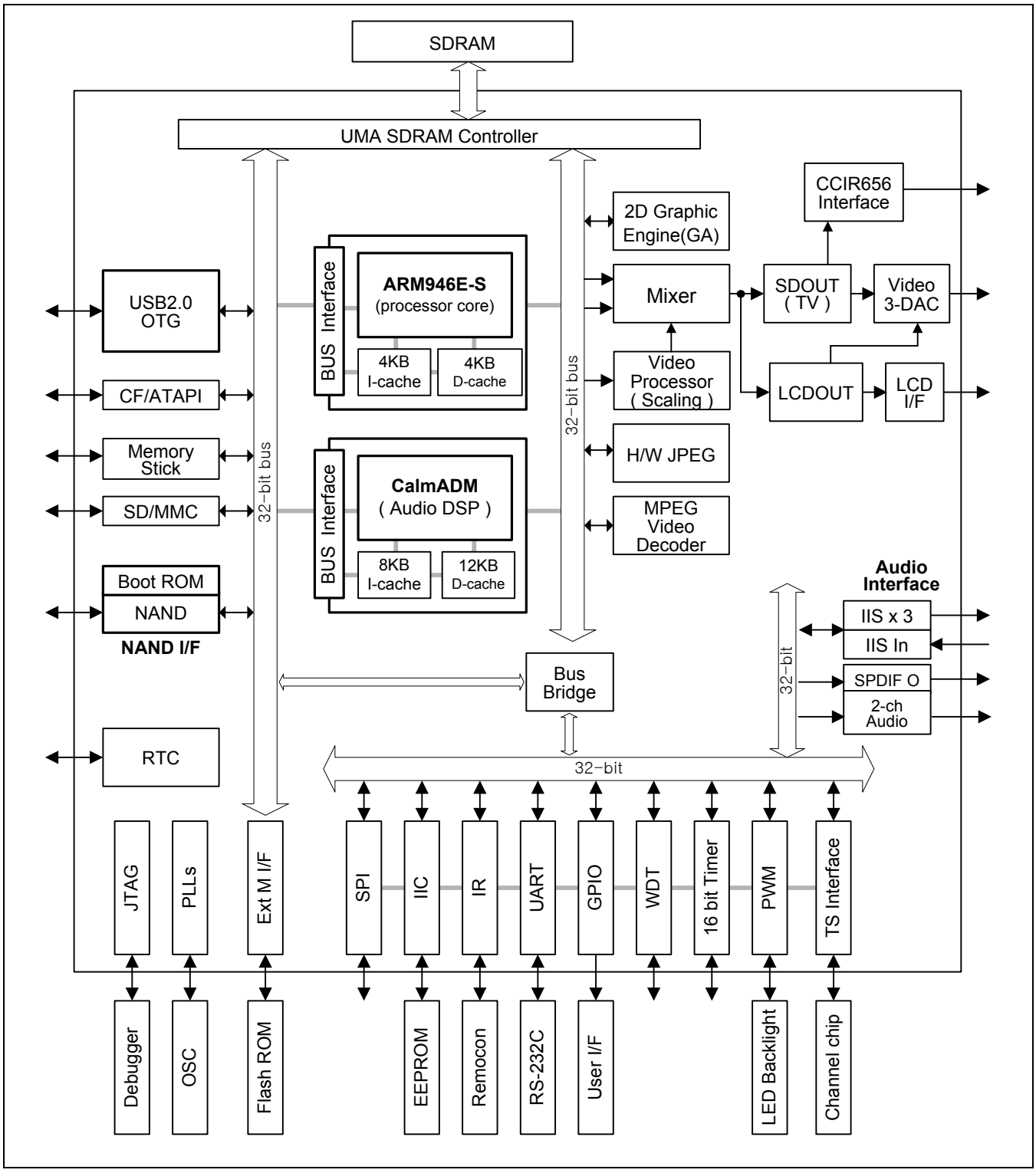

Figure 1-1. S5L2010 Block Diagram

COMPARISON TABLE

Feature	S5L2010F	S5L2010D	S5L2010A	S5L5025(DVD)
Process	65n	65n	65n	65n
Core	ARM9	ARM9	ARM9	ARM7
Core Speed	176MHz	176MHz	176MHz	132MHz
OS	iRTOS	iRTOS	iRTOS	iRTOS
Video Codec	MPEG1/2/4	MPEG1/2/4	MPEG1/2/4	MPEG1/2/4
LCD Interface	**Analog/Digital**	**Digital(RGB 18-bit)**	**Analog**	**X**
TCON Include	O	O	O	X
Decoding width (JPEG)	**65536 x 65536**	**65536 x 65536**	**65536 x 65536**	**4096 x 4096**
Decoding Speed (JPEG)	**57Mpixel/sec**	**57Mpixel/sec**	**57Mpixel/sec**	**1.5Mpixel/sec**
Display Performance	1024 x 768	1024 x 768	1024 x 768	800 x 576
Display Effect	Various	Various	Various	Simple
NAND Booting	**SLC/MLC**	**SLC/MLC**	**SLC/MLC**	**X**
SD Card Booting	**O**	**O**	**O**	**X**
Memory Card I/F	CF/SD/MMC/MS/xD	CF/SD/MMC/MS/xD	CF/SD/MMC/MS/xD	SD, MMC, MS
Video DAC(TV Output)	3	0	3	4
Audio Channel (PWM)	2	2	2	2
IIS Output Channel	6	6	6	X
IIS Input Channel	2	2	2	X
TS Interface	O	O	O	X
RTC	O	O	O	X
ADC	12-bit 7-ch	12-bit 4-ch	12-bit 4-ch	14-bit 1-ch
USB	USB2.0 OTG	USB2.0 OTG	USB2.0 OTG	USB1.1 Host
LVD RESET	O	O	O	O
Flash memory I/F	Serial	Serial	Serial	Serial
PAD Power	3.3V	3.3V	3.3V	3.3V
Core Power	1.2V	1.2V	1.2V	1.2V
Internal BUS Clock (ARM, ADM, Bus)	132MHz	132MHz	132MHz	132MHz
SDRAM Clock (Max)	132MHz	132MHz	132MHz	132MHz
Minimum SDRAM	16Mbit	16Mbit	16Mbit	16Mbit
Package	**160-LQFP**	**128-eTQFP**	**128-eTQFP**	**128-QFP**

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HotTel:+86-21-58998693

FEATURES

RISC Processor Architecture

- ARM946E-S based core processor
- Fully 16/32-bit RISC architecture.
- 4KB/4KB Instruction and Data separated cache
- Up to 176 MHz operating frequency

Cache Memory

- 64 way set-associative cache with I-cache(4KB) and D-cache(4KB)
- 8-word per line with one valid bit and two dirty bits per line
- Pseudo random or round robin replacement algorithm
- Write through or write back cache operation to update the main memory
- The write buffer can hold 8 words of data and four address

Memory Controller

- Supports 1/2-bit serial flash interface.
- Supports 4/8-bit EDO-DRAM interface
- Supports 16-bit data bus width for SDR interface
- SDRAM usage.
  – 16Mbit SDRAM x1 (2-bank).
  – 16Mbit SDRAM x2 (4-bank).
  – 64/128Mbit SDRAM x1 (4-bank)
- Fully Programmable access cycles for all memory banks.

JPEG Decoder

- Decoded ITU-T.81 (ISO/IEC 10918-1) compliant baseline process.
- Decode up to maximum 65535x65535 pixel size
- Operation Clock Frequency : 132 MHz
- Support variable JPEG image chroma format
- Fine zoom operation with small memory (under 1MB)

MPEG Video Decoder

- Decodes MPEG1, MPEG2 (MP@ML) and MPEG4 ASP video stream
- Error detection and autonomous error concealment
- Provides a programmable core for robust decoding of various MPEG4 stream
- Decodes images having max. width of 960
- Decodes MPEG1, MPEG2 video stream (MP@ML)

Audio Stream Decoder

- Decodes MPEG1, MPEG2, OGG, AAC and WMA.
- Supports down mix
- CalmMAC24 for audio signal processing
  – 24-bit high performance fixed-point DSP co-processor, 24x24 MAC operation in 1 cycle
  – 2 multiplier accumulator registers, 4 general accumulator registers, and 8 pointer registers

LCD I/F

- Horizontal max. size : 1024 ,
  Vertical max. size : 768
- Supported MCU Interface
  - 6800 MCU Interface with 18/16/8 bit parallel interface.
  - 8080 MCU Interface with 18/16/8 bit parallel interface.
- Supported LCD Interface
  - Analog LCD Interface.
  - Digital LCD Interface with RGB 18-bit.
  - Digital LCD Interface with 8bit RGB.
- Supported DDI Interface
  - Analog Source DDI + Gate DDI
  - Digital Source DDI (Only TTL) + Gate DDI

12-bit ADC & Touch Screen I/F

- Resolution: 12-bit
- Maximum conversion rate: 1MSPS
- Power supply: 3.3V (Typ.), 1.2V (Typ.)
- Touch screen function (4-wire resistive touch).

FEATURES (CONTINUED)

Video Processor (VP)

- Source resolution: Max 1024x768
- Output Resolution: Max 1024x768
- Aspect ratio conversion
  Letterbox / Pan & Scan
- De-interlacing
  – Weave: For film source
  –IPC: For interlaced video
- Slide show : wipe diagonal +, wipe diagonal –, wipe horizontal, wipe vertical
- fade in/out, dissolve
- Zoom In/Out: 16x – 1/4 Display format
-

Graphic Accelerator (GA) & Mixer

- 3 graphic layers & 2 video layers : YCbCr format
  Graphic Layer1 : 1/2/4/8-bpp (sub OSD)
  Graphic Layer2 : 4/8/16/32-bpp (main OSD)
  Graphic Layer3 : 4-bpp (sub-picture , cursor)
  Video Layer1-2 : supports image effects
- Supports Layer Blending
  – Arbitrary priority control of graphic and video layer
  – 256 level alpha blending (graphic to video layer, pixel to video layer)
- Supports display maximum size 1024x768
- Support two 256x32bit palette for graphic layer and one 16x16bit palette for cursor layer
- Supports image effects
  – sliding, corner sliding, translation, rollup, rolling, bars, snail, stairs, square, grid, fading, cross comb, shutter

NTSC/PAL Encoder & Video Output

- 3CH 10-bit Video DACs(Analog output)
  – YPbPr, RGB, CVBS, YC output.
- CCIR-656 compatible digital output

RTC (Real Time Clock)

- Full clock features: msec, sec, min, hour, day, week, month, year
- 32.768 KHz operation
- Alarm interrupt (no wake function)

Watchdog Timer

- 16-bit Watchdog Timer.
- Interrupt request or system reset at time-out.

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Timers and PWM

- 16-bit Timer 1, 2
  – Interval, free run, one shot and capture mode
  – Programmable duty cycle,frequency and polarity.
- 16-bit Timer 3, 4
  – Interval mode and free run mode
  – Supports external clock source.
- High speed PWM1, PWM2 and PWM3
  – Interval, free run, one shot and capture mode
  – PWM function for LED backlight.
- 32-bit Timer : free run mode

Interrupt Controller

- Various Interrupt sources
  (Watch dog timer, 7 Timers, UART, 8 External interrupts, I2C, I2S, SPI, IR, SPDIFOUT, Mstick, SDCI etc.)
- Edge detect mode on external interrupt source.
- Programmable polarity of rising and falling.
- Supports FIQ (Fast Interrupt request) for very urgent interrupt request.

SPDIF Interface

- Integrated IEC60958 encoder (SPDIF output)
- 2x8 bits Shift register for transmit.
- DMA-based or interrupt-based operation.

I2S Audio In/Out (3ch output, 1ch input)

- 3-channel I2S-bus for audio interface with DMA-based operation (6 digital channel)
- 1-channel I2S input for Mic input
- Serial, 8/16/24bit per channel data transfers
- Up to 24-bit sample size, up to 192KHz sample

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HotTel:+86-21-58998693

FEATURES (Continued)

IR Input

- Supports consumer electronic IR protocol

SPI

- Transmit and receive the 8 bit data in the simple manner
- SPI protocol (ver 2.11) compatible

I2C Interface

- 1-channel Multi-Master I2C-Bus.
- Serial, 8-bit oriented and bi-directional data transfers can be made at up to 100 Kbit/s (standard mode) or up to 400 Kbit/s (fast mode)

UART

- UART with DMA-based or interrupt-based operation
- Supports 5-, 6-, 7-, or 8-bit serial data transmit/receive
- Supports H/W handshaking during transmit/receive
- Programmable baud rate
- Loop back mode for testing
- Internal 16-byte Tx FIFO and 16-byte Rx FIFO

Memory Card Interface (All-in-1)

- Memory Stick (Standard ver1.4, Pro ver1.0)
- SD ver2.0 / MMC ver 4.1
- CF ver4.1
- xD ver1.2 / Smart Media ver2003

NAND Flash Interface

- NAND Flash Interface with x8 data bus
- Supports SLC/MMC NAND (up to 8-bit ECC)

NAND Flash Boot Loader

- System can be booted from NAND when system initialization begins
- Supports both SLC and MLC NAND Flash memory

.

USB2.0 OTG

- USB 2.0 OTG supporting high speed (480Mbps, on-chip transceiver).

Channel I/F

- Support TS interface in DVB-H/DVB-T/ISDB-T/ T-DMB/DAB mode
- I/F Signal (TS_CLK, TS_DATA, TS_VALID, TS_SYNC, TS_ERROR)

Clock & Power Manager

- Low power consumption
- On-chip PLLs
- Clock can be fed selectively to each function block under software control
- Power mode : Normal, Stop mode.
  Normal mode: Normal operating mode.
  Stop mode : All clocks are stopped.

Oscillator

- Single 24MHz crystal clock input.
- Oscillation Sources & PLL

Operating Voltage

- Core: 1.2V
- I/O: 3.3V

Operating Temperature

- 0°C – 70 °C

Operating Frequency

- Up to 176 MHz

Package

- S5L2010F : 160-LQFP-2424
  S5L2010A : 128-eTQFP-1414
  S5L2010D : 128-eTQFP-1414

S5L2010 BASED DPF SYSTEM DIAGRAM

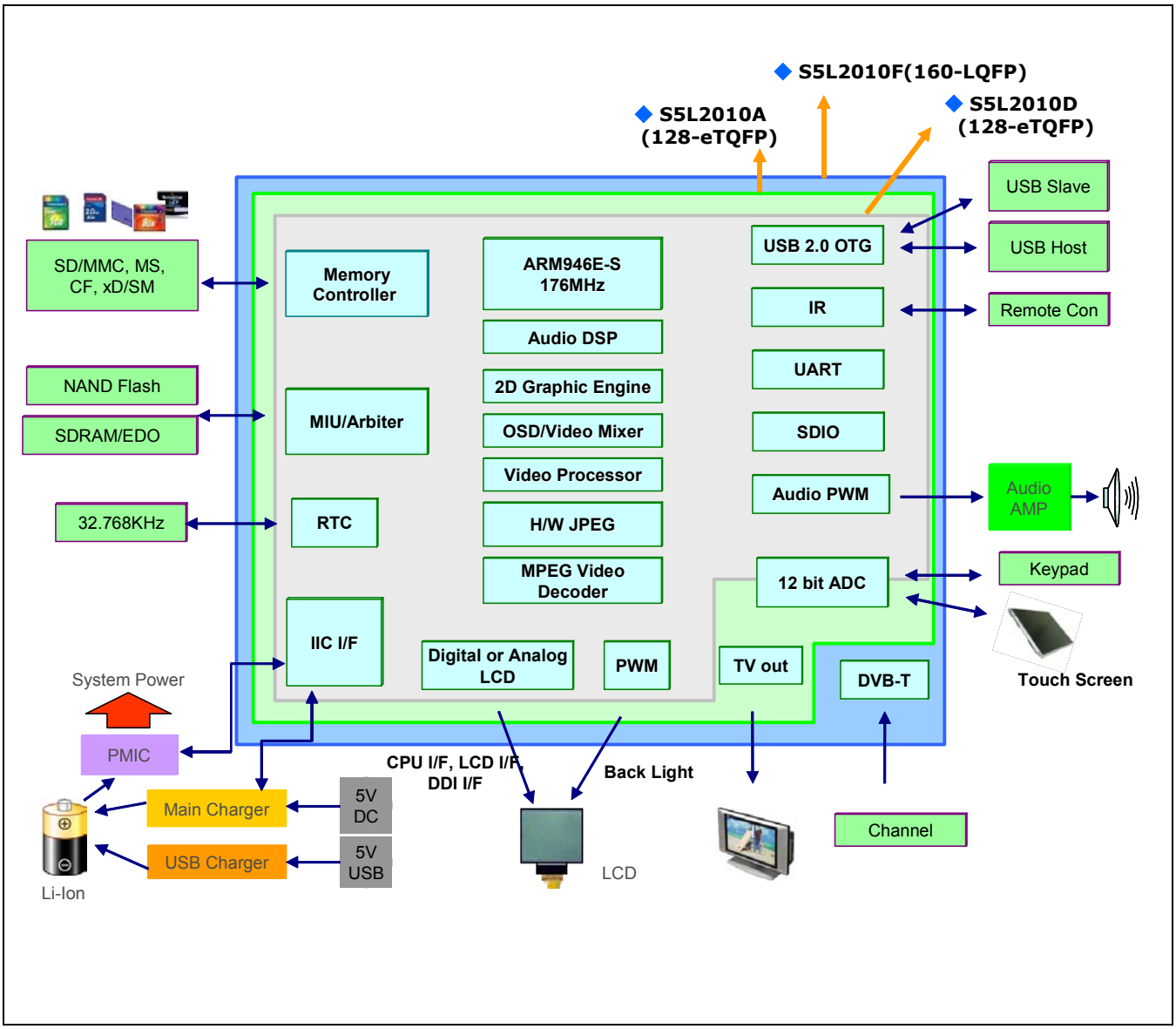

Figure 1-2. System Diagram

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MEMORY ADDRESS MAP

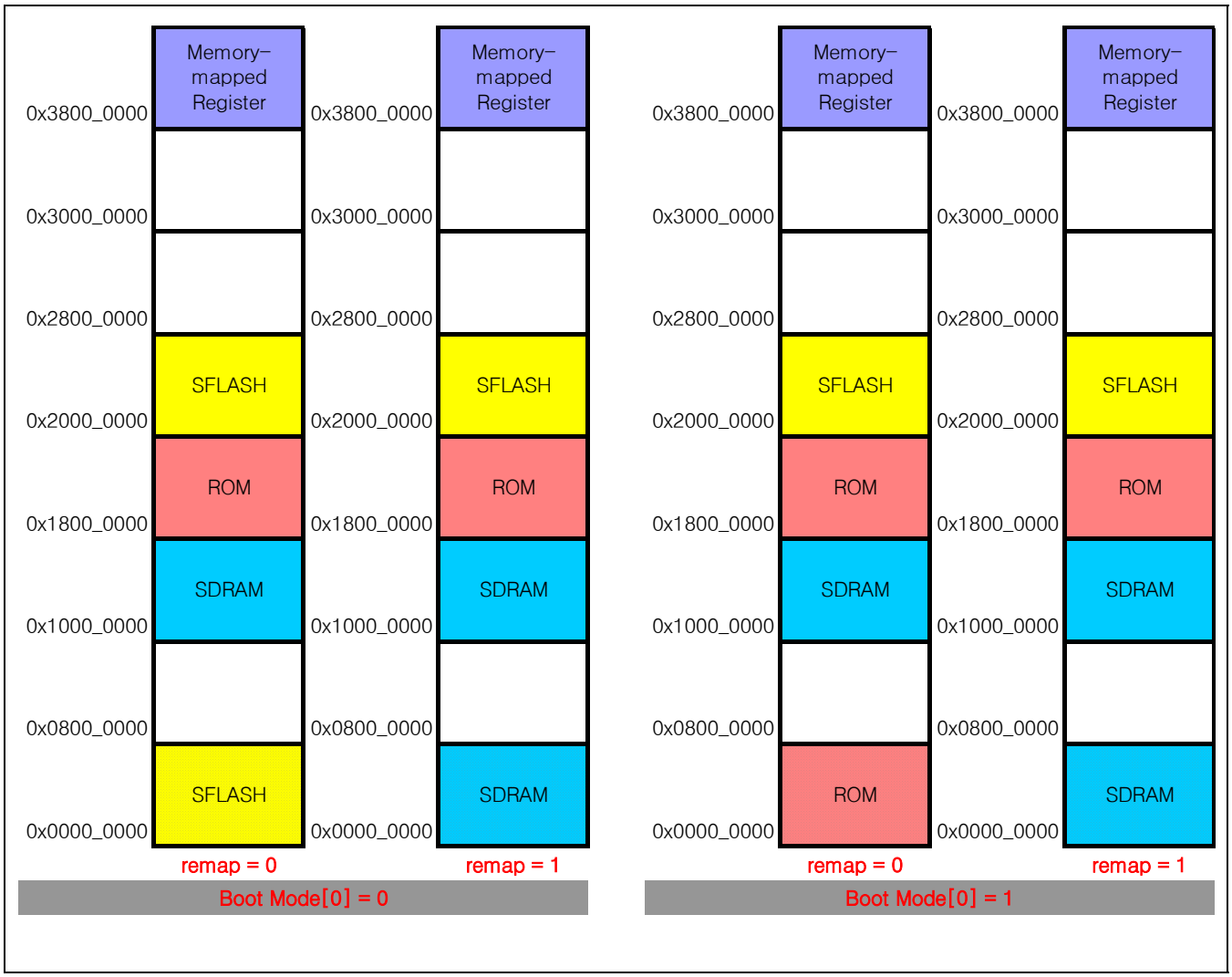

Figure 1-3. Available Address Space of S5L2010

2010 has a memory configuration shown in figure. SDRAM, Flash, Boot ROM memory and internal registers are mapped in the address space of 0x0000_0000 ~ 0x3FFF_FFFF.

#	IP	Base Address
1	MIU	0x3820_0000
2	IODMA	0x3840_0000
3	BAT	0x3860_0000
4	LCD_VP	0x3880_0000
5	MIXER	0x38A0_0000
6	CSCR	0x38C0_0000
7	LCD_OUT	0x38E0_0000
8	ADM	0x3900_0000
9	CF_IF	0x3920_0000
10	MPVD	0x3940_0000
11	TSI	0x3960_0000
12	GA	0x3980_0000
13	SDOUT	0x39A0_0000
14	ICU	0x39C0_0000
15	ECC	0x39E0_0000
16	CSDMA	0x3A00_0000
17	JPEG	0x3A20_0000
18	FCSCALER	0x3A40_0000
19	Reserved	0x3A60_0000
20	USB2.0(OTG)	0x3A80_0000
21	NAND_FLASH	0x3AA0_0000

#	IP	Base Address
22	RTC	0x3C00_0000
23	PWM	0x3C10_0000
24	SDCI	0x3C20_0000
25	APU_ADM	0x3C30_0000
26	IR	0x3C40_0000
27	CLKGEN	0x3C50_0000
28	MSTICK	0x3C60_0000
29	TIMER	0x3C70_0000
30	WDT	0x3C80_0000
31	I2C	0x3C90_0000
32	I2S	0x3CA0_0000
33	SPDIFOUT	0x3CB0_0000
34	UART1	0x3CC0_0000
35	SPI	0x3CD0_0000
36	TIME_STAMP	0x3CE0_0000
37	GPIO	0x3CF0_0000
38	UART2	0x3D00_0000
39	Reversed	0x3D10_0000
40	Reserved	0x3D20_0000
41	ADC_CON	0x3D30_0000
42	Reversed	0x3D40_0000
43	APU_MPVD3	0x3D50_0000
44	APU_MPVD4	0x3D60_0000
45	JOG	0x3D70_0000
46	PG	0x3D80_0000
47	SPDIFIN	0x3D90_0000
48	USB2.0(OTG)	0x3DA0_0000

Figure 1-4. Base Address of memory mapped IP

.

BOOT MODE

The S5L2010 DPF SOC can be booted from NAND or Flash memory when system initialization begins. Configuration mode is selected Boot1, Boot0 pin status.

Boot 1	Boot 0	Available JTAG	Configuration Mode
0	0	Case1 : Port 3	Serial Flash Booting
0	1	Case2 : Port 0	Internal ROM Booting (NAND Flash or SD Card)
1	0	–	Test
1	1	–	

Debugging environment (JTAG)

The S5L2010 DPF SoC has 2 JTAG ports. The ARM core processor can be controlled through its JTAG port.

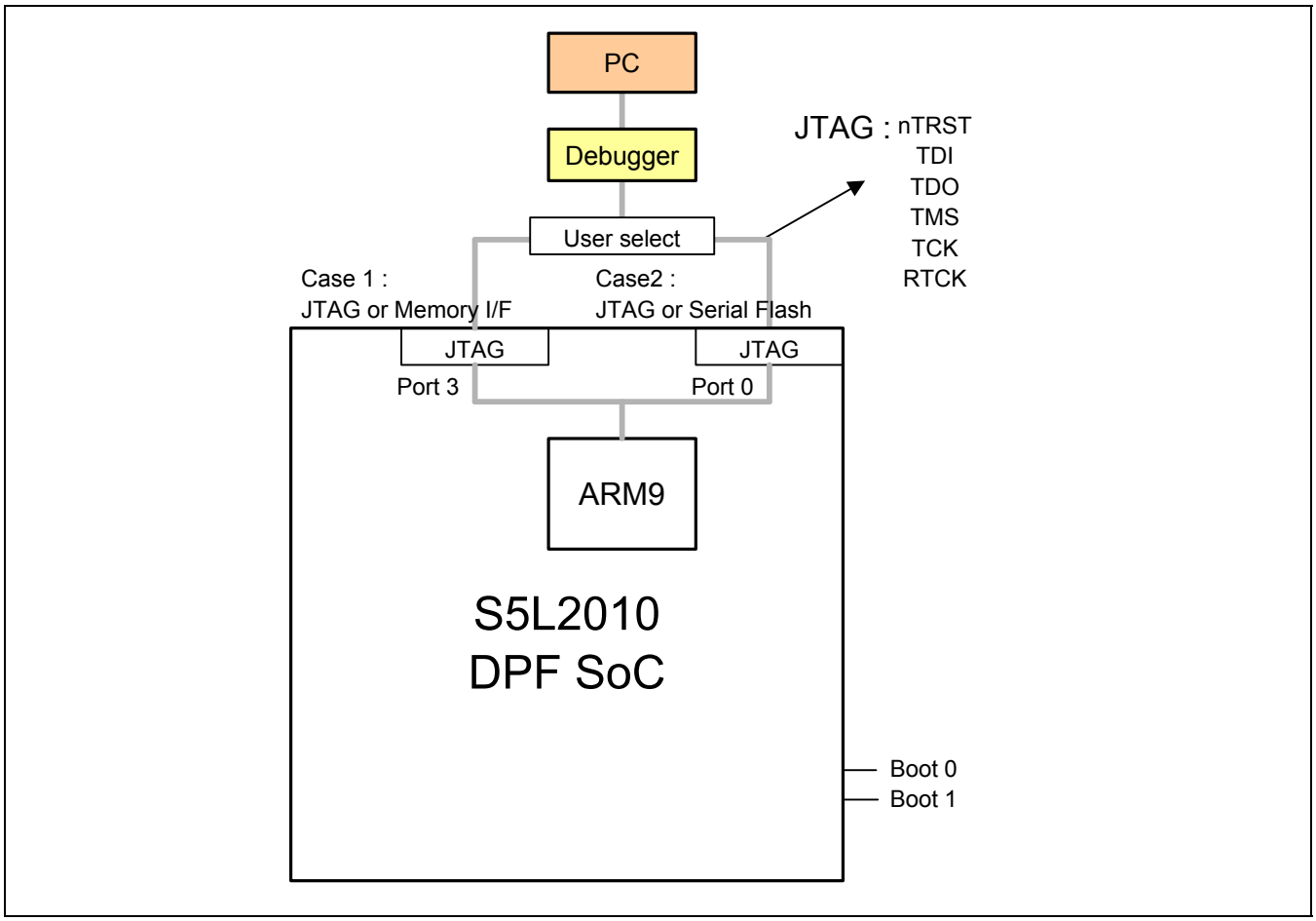

Figure 1-5. JTAG Interface

PIN ASSIGNMENT

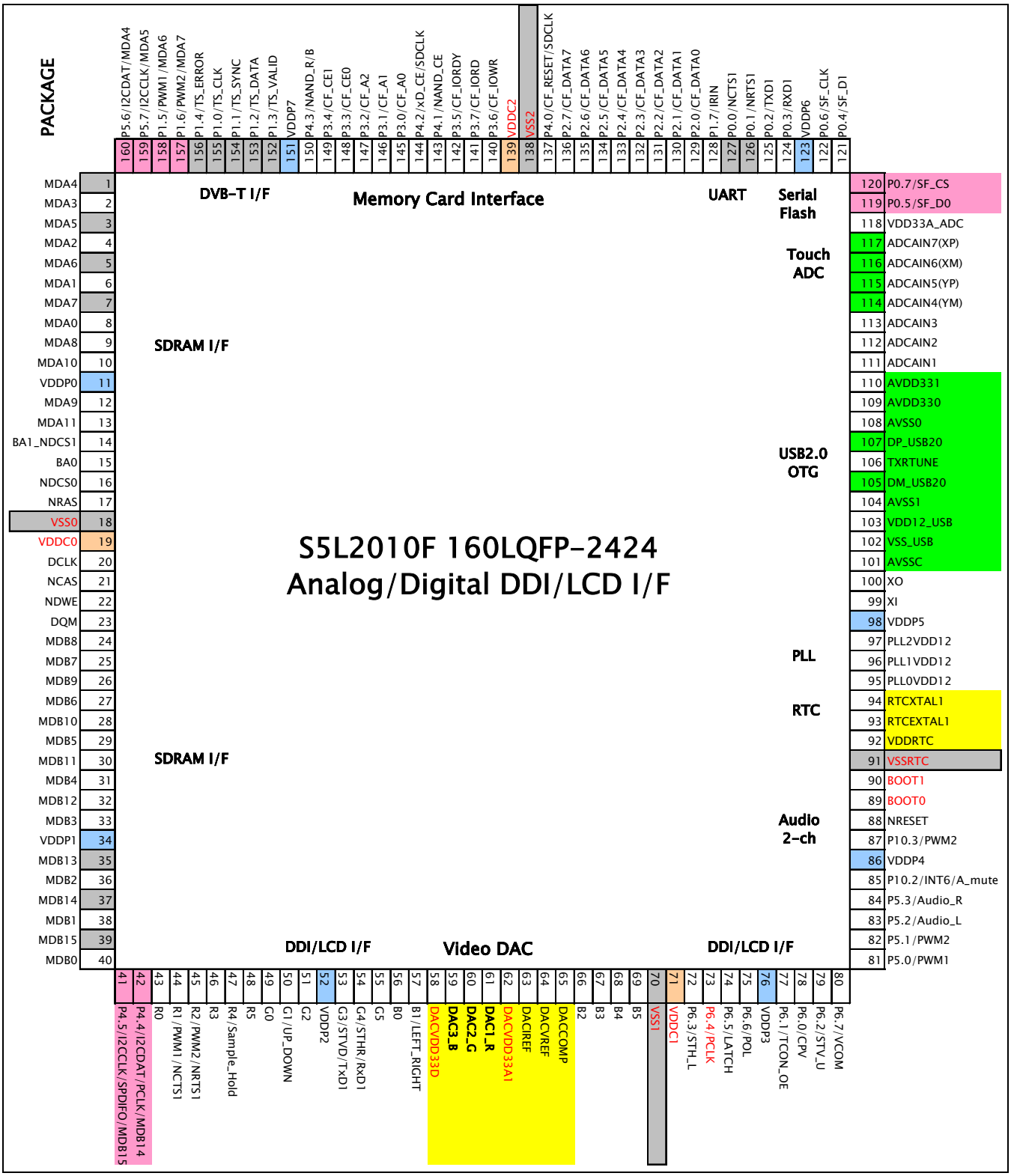

Figure 1-6. S5L2010F Pin Assignments (160-LQFP-2424)

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HotTel:+86-21-58998693

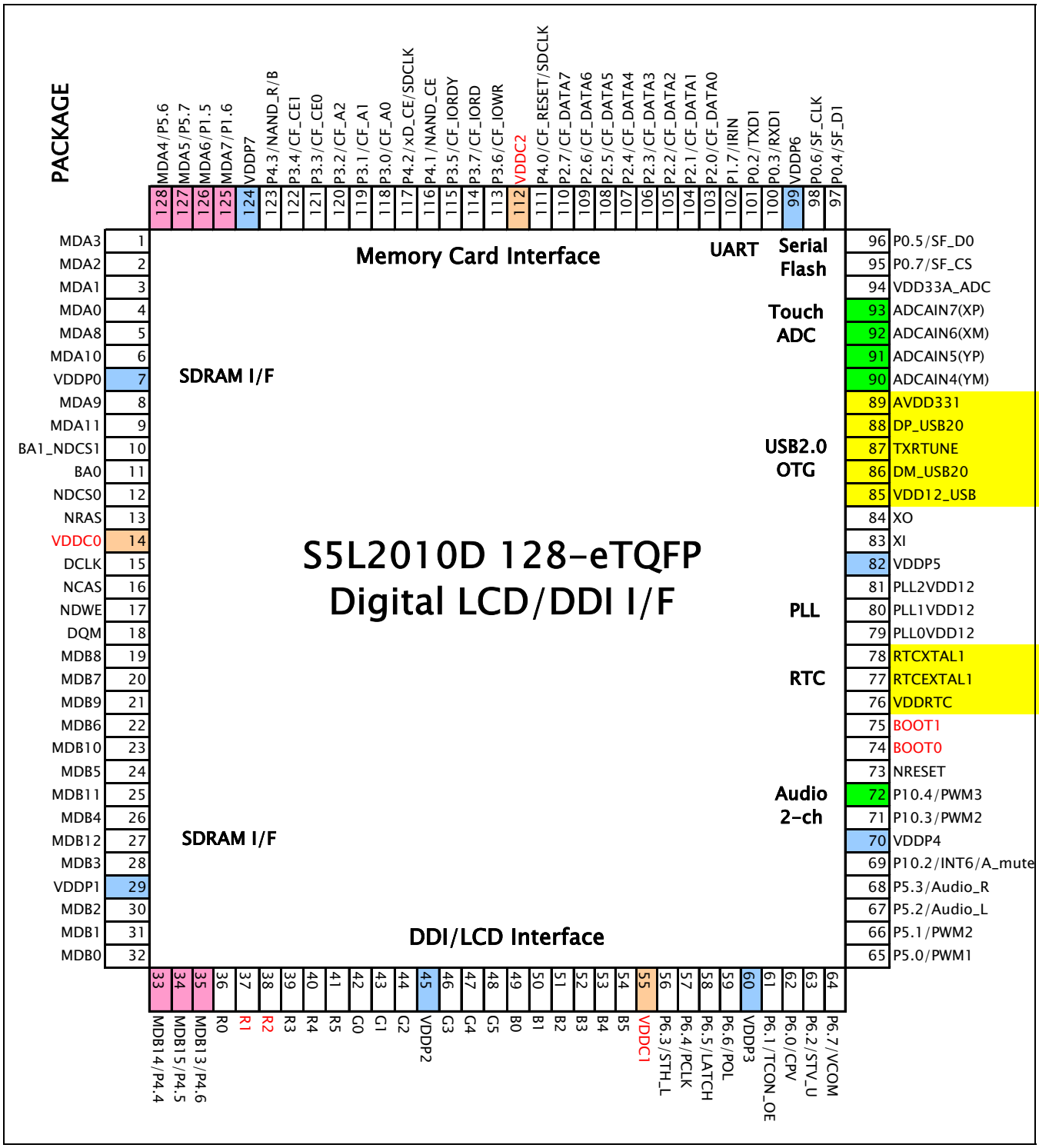

Figure 1-7. S5L2010D Pin Assignments (128-eTQFP-1414)

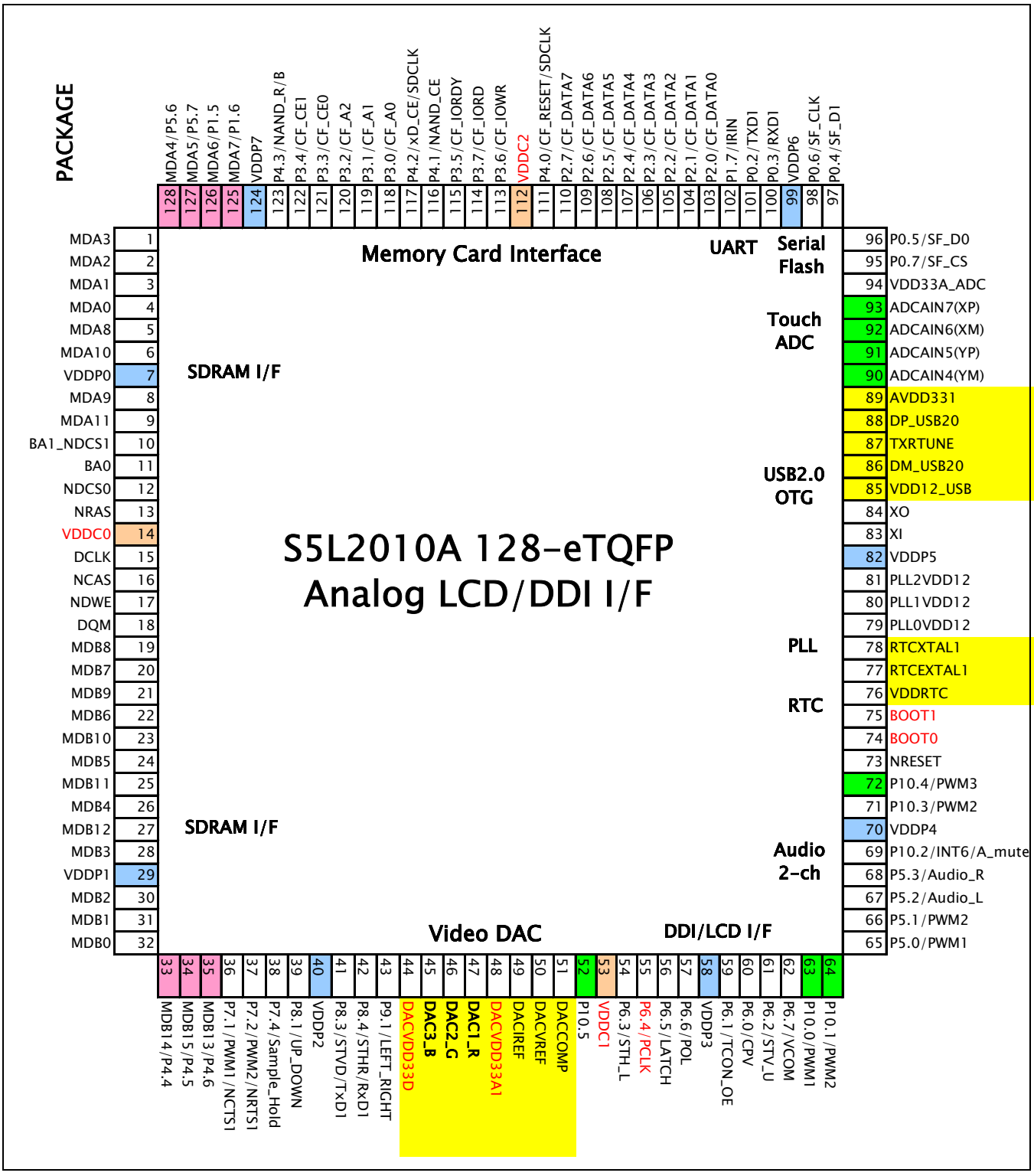

Figure 1-8. S5L2010A Pin Assignments (128-eTQFP-1414)

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GPIO TABLE

PORT			Func0	Func1	Func2		Func3		Func4		Func5		Func6		Func7		Func8	
128D핀	128A핀	160핀	Name	Name	Name	I/O	Name	I/O	Name	I/O	Name	I/O	Name	I/O	Name	I/O	Name	I/O
		127	P0.0	INT0	output		NCTS1	I	TxD2	O	TAOUT(PWM)	O	EMG1	I	STV_D	O	TACAP	I		
		126	P0.1	input	output		NRTS1	O	RxD2	I	TBOUT(PWM)	O	EMG2	I	UD	O	TBCAP	I		
101	101	125	P0.2	input	output		TXD1	O	**NTRST**	**I**	PWM1	O	EMG3	I	STH_R	**O**	IIS_IN	I		
100	100	124	P0.3	INT7	output		RXD1	I	**TDI**	**I**	IRIN	I	**PWM3**	**O**	LR	O	IIS_DAT0	O		
97	97	121	P0.4	input	output		SF_D1	B	**TDO**	**O**	PWM1	O	NCTS1	I			IISLRCK	O		
96	96	119	P0.5	input	output		SF_D0	B	**TMS**	**I**	PWM2	O	NRTS1	O			IISBCLK	O		
98	98	122	P0.6	input	output		SF_CLK	O	**RTCK**	**O**	CKO	O	TACLK	I			**IISMCLK**	O	NRTS1	O
95	95	120	P0.7	input	output		**SF_CS**	O	**TCK**	**I**										
		155	P1.0	input	output		PWM1	O	TxD1	O	TS_CLK	I	PG0	O	SPICLK	B	nPWM1	O	CF_DATA[8]	B
		154	P1.1	input	output		PWM2	O	NCTS2	I	TS_SYNC	I	PG1	O	MOSI	B	nPWM2	O	CF_DATA[9]	B
		153	P1.2	input	output		PWM3	O	NRTS2	O	TS_DATA	I	PG2	O	MISO	B	nPWM3	O	CF_DATA[10]	B
		152	P1.3	INT1	input	output	TAOUT(PWM)	O	TxD2	O	TS_VALID	I	PG3	O			TxD2	O	CF_DATA[11]	B
		156	P1.4	INT2	output		TBOUT(PWM)	O	TACLK	I	TS_ERROR	I	PG4	O			RxD2	I	CF_DATA[12]	B
126	126	158	P1.5	input	output		PWM1	O	MDA6	O	SPICLK	B	PG5	O					CF_DATA[13]	B
125	125	157	P1.6	input	output		PWM2	O	MDA7	O	MOSI	B	PG6	O	SPDIFO	O			CF_DATA[14]	B
102	102	128	P1.7	input	output		**PWM3**	**O**	IRIN	I	MISO	B	PG7	O	CKO	O	RTCOSC	O		
103	103	129	P2.0	input	output	CF_DATA[0]	B	IO[0]	B	**DAT[0]**	**B**	**DIO[0]**	**B**							
104	104	130	P2.1	input	output	CF_DATA[1]	B	IO[1]	B	**DAT[1]**	**B**	**DIO[1]**	**B**							
105	105	131	P2.2	input	output	CF_DATA[2]	B	IO[2]	B	**DAT[2]**	**B**	**DIO[2]**	**B**							
106	106	132	P2.3	input	output	CF_DATA[3]	B	IO[3]	B	**DAT[3]**	**B**	**DIO[3]**	**B**					NTRSTADM	I	
107	107	133	P2.4	input	output	CF_DATA[4]	B	IO[4]	B	**DAT[4]**	**B**							TDOADM	O	
108	108	134	P2.5	input	output	CF_DATA[5]	B	IO[5]	B	**DAT[5]**	**B**							TDIADM	I	
109	109	135	P2.6	input	output	CF_DATA[6]	B	IO[6]	B	**DAT[6]**	**B**							TMSADM	I	
110	110	136	P2.7	input	output	CF_DATA[7]	B	IO[7]	B	**DAT[7]**	**B**							TCKADM	I	
118	118	145	P3.0	input	output	CF_A0	O	CLE	O			TS_CLK	I					**NTRST**	**I**	
119	119	146	P3.1	input	output	CF_A1	O	ALE	O	NCTS2	I	TS_SYNC	I					**TDI**	**I**	
120	120	147	P3.2	input	output	CF_A2	O	RE	O	NRTS2	O	TS_DATA	I					**TDO**	**O**	
121	121	148	P3.3	input	output	CF_CE0	O	WE	O	RxD2	I	TS_VALID	I					**TMS**	**I**	
122	122	149	P3.4	input	output	CF_CE1	O			TxD2	O	TS_ERROR	I	PWM1	O			**TCK**	**I**	
115	115	142	P3.5	input	output	**CF_IORDY**	**I**	R/B0	I											
113	113	140	P3.6	input	output	**CF_IOWR**	**O**	R/B1(xD)	I									**RTCK**	**O**	
114	114	141	P3.7	input	output	**CF_IORD**	**O**			**CMD0**	**B**	BS	O							
111	111	137	P4.0	input	output	**CF_RESET**	**O**			**CLK0**	**O**			PWM2	O			PG0	O	
116	116	143	P4.1	input	output			**CE0**	**O**									PG1	O	
117	117	144	P4.2	input	output			**CE1(xD)**	**O**	**CLK0**	**O**	**SCLK**	**O**					PG2	O	
123	123	150	P4.3	input	output	MDA12	O	R/B0	I									PG3	O	
33	33	42	P4.4	input	output	I2CDAT	B	MDB14	B	**JOG1**	**I**	EMG1	I	nRST_LCD	O	PCLK	O			
34	34	41	P4.5	input	output	I2CCLK	B	MDB15	B	JOG2	I	EMG2	I	**Ext_LCD_Int**	I	SPDIFO	O			
35	**35**		P4.6	INT3	output	PWM1	O	MDB13	B	PCLK	O			**Ext_LCD_Int**	I					
65	65	81	P5.0	input	output	PWM1	O													
66	66	82	P5.1	INT5	output	PWM2	O													
67	67	83	P5.2	input	output	PWM0_L_REG	O	PWM0_L	O											
68	68	84	P5.3	input	output	PWM0_R_REG	O	PWM0_R	O											
10	10	14	P5.4	input	output	BA1_nDCS1	O													
9	9	13	P5.5	input	output	MDA11	O													
128	128	160	P5.6	input	output	MDA4	O	I2CDAT	B	**JOG1**	**I**	TxD2	O							
127	127	159	P5.7	input	output	MDA5	O	I2CCLK	B	JOG2	I	RxD2	I							CF_DATA[15]	B

					LCD(Digital)		LCD(Analog)		TCON(Digital)		TCON(Analog)		CPU IF					
PORT			Func0	Func1	Func2		Func3		Func4		Func5		Func6		Func7		Func8	
128D핀	128A핀	160핀	Name	Name	Name	I/O	Name	I/O	Name	I/O	Name	I/O	Name	I/O	Name	I/O	Name	I/O
62	60	78	P6.0	input	output	PWM1	O	TS_CLK	I	CPV	O	CPV	O	CPU_CS	O	VDAT0	O	IISMCLK	O
61	59	77	P6.1	input	output	DE	O	TS_SYNC	I	OE	O	OE(OEV)	O			VDAT1	O	IISBCLK	O
63	61	79	P6.2	input	output	PWM1	O	TS_DATA	I	STV_U	O	STV_U	O	CPU_RS	O	VDAT2	O	IISLRCK	O
56	54	72	P6.3	input	output	PWM2	O	TS_VALID	I	STH_L	O	STH_L	O	CPU_RD	O	VDAT3	O	IIS_DAT0	O
57	55	73	P6.4	input	output	PCLK	O	TS_ERROR	I	PCLK	O	R_CLK	O			VDAT4	O	IIS_DAT1	O
58	56	74	P6.5	input	output	H-Sync	O	H-Sync	O	LATCH	O	G_CLK	O			VDAT5	O	IIS_DAT2	O
59	57	75	P6.6	input	output	V-Sync	O	V-Sync	O	POL	O	B_CLK	O	CPU_V-Sync	O	VDAT6	O		
64	62	80	P6.7	INT4	output	PWM2	O	SPDIFO	O	VCOM	O	VCOM	O	WR	O	VDAT7	O		
36		43	P7.0	input	output	R0	O			R0	O			D1	B	BTCLK	O		
37	36	44	P7.1	input	output	R1	O	PWM1	O	R1	O	MODE1	O	D2	B	NCTS1	I		
38	37	45	P7.2	input	output	R2	O	PWM2	O	R2	O	MODE2	O	D3	B	NRTS1	O	CF_DATA[8]	B
39		46	P7.3	input	output	R3	O	X		R3	O	X		D4	B			CF_DATA[9]	B
40	38	47	P7.4	input	output	R4	O	SPDIFO	O	R4	O	Sample&Hold	O	D5	B				
41		48	P7.5	input	output	R5	O	X		R5	O	X		D6	B			CF_DATA[10]	B
42		49	P8.0	input	output	G0	O			G0	O			D7	B				
43	39	50	P8.1	input	output	G1	O	SPDIF_IN	I	G1	O	UD	O	D8	B				
44		51	P8.2	input	output	G2	O	X		G2	O	X		D9	B			CF_DATA[11]	B
46	41	53	P8.3	input	output	G3	O	TxD1	O	G3	O	STV_D	O	D10	B	JOG1	I	CF_DATA[12]	B
47	42	54	P8.4	input	output	G4	O	RxD1	I	G4	O	STH_R	O	D11	B	JOG2	I	CF_DATA[13]	B
48		55	P8.5	input	output	G5	O	X		G5	O	X		D12	B			CF_DATA[14]	B
49		56	P9.0	input	output	B0	O	JOG1	I	B0	O			D13	B				
50	43	57	P9.1	input	output	B1	O	JOG2	I	B1	O	LR	O	D14	B				
51		66	P9.2	input	output	B2	O	X		B2	O	X		D15	B			CF_INTREQ	I
52		67	P9.3	input	output	B3	O	X		B3	O	X		D16	B			CF_DATA[15]	B
53		68	P9.4	input	output	B4	O	X		B4	O	X		D17	B			CF_DMACK	O
54		69	P9.5	input	output	B5	O	X		B5	O	X		D18	B			CF_DMAREQ	I
	63		P10.0	input	output	PWM1	O												
	64		P10.1	input	output	PWM2	O					PG1	O						
69	69	85	P10.2	INT6	output	TxD2	O	JOG1	I	I2CDAT	B	PG0	O	Auto_mute	O				
71	71	87	P10.3	input	output	RxD2	I	JOG2	I	I2CCLK	B	TBCLK	I	PWM2	O	Auto_mute	O		
72	72		P10.4	input	output							SPDIFO	O	**PWM3**	**O**				
	52		P10.5	input	output														

PIN DESCRIPTION

Table 1-1. S5L2010F/D/A Pin Descriptions

Pin name	I/O	Description	S5L2010F 160-LQFP		S5L2010D 128-eTQPF		S5L2010A 128-eTQPF	
			GPIO	PIN	GPIO	PIN	GPIO	PIN
System								
NRESET	B	Global reset input when LVD is disabled. Global reset output when LVD is enabled. (active low)	–	88	–	73	–	73
XI	I	27MHz Oscillator clock input, or crystal input	–	99	–	83	–	83
XO	O	Oscillator out to connected to XI, If no crystal used, must be left NC.	–	100	–	84	–	84
BOOT1	I	Boot mode control 1	–	90	–	75	–	75
BOOT0	I	Boot mode control 0	–	89	–	74	–	74
CKO	O	PLLs Clock out for test	P0.6	122	P0.6	98	P0.6	98
			P1.7	128	P1.7	102	P1.7	102
RTC			S5L2010F		S5L2010D		S5L2010A	
RTCXTAL1	O	RTC Crystal output	–	94	–	78	–	78
RTCEXTAL1	I	RTC Crystal Input	–	93	–	77	–	77
VDDRTC	P	RTC power(3.3V)	–	92	–	76	–	76
VSSRTC	P	RTC ground	–	91	–	–	–	–
ARM9 Debugger			S5L2010F		S5L2010D		S5L2010A	
NTRST	I	Tap controller reset (active low) for ARM JTAG.	P0.2	125	P0.2	101	P0.2	101
			P3.0	145	P3.0	118	P3.0	118
TDI	I	Test data input for ARM JTAG	P0.3	124	P0.3	100	P0.3	100
			P3.1	146	P3.1	119	P3.1	119
TDO	O	Test data output for ARM JTAG	P0.4	121	P0.4	97	P0.4	97
			P3.2	147	P3.2	120	P3.2	120
TMS	I	Tap controller Machine State control for ARM JTAG	P0.5	119	P0.5	96	P0.5	96
			P3.3	148	P3.3	121	P3.3	121
TCK	I	ARM JTAG Clock Input	P0.7	120	P0.7	95	P0.7	95
			P3.4	149	P3.4	122	P3.4	122
RTCK	O	ARM debug sync clock	P0.6	122	P0.6	98	P0.6	98
			P3.6	140	P3.6	113	P3.6	113
ADM Debugger			S5L2010F		S5L2010D		S5L2010A	
NTRSTADM	I	Tap controller reset (active low) for ADM JTAG	P2.3	132	P2.3	106	P2.3	106
TDOADM	O	Test data output for ADM JTAG	P2.4	133	P2.4	107	P2.4	107
TDIADM	I	Test data input for ADM JTAG	P2.5	134	P2.5	108	P2.5	108
TMSADM	I	Tap controller Machine State control for ADM JTAG	P2.6	135	P2.6	109	P2.6	109
TCKADM	I	ADM JTAG Clock Input	P2.7	136	P2.7	110	P2.7	110

Email:Tech@fosvos.com
HotTel:+86-21-58998693